

**Specification Amendment**

Please re-write the first full paragraph starting on page 11 as follows:

--Figure 4 illustrates a block diagram of master delay 400 in an exemplary embodiment of the invention. Master delay 400 may be suitable for use as master delay circuit 201 of Figure 2. Master delay 400 includes delay unit 401 and monitor logic 408. Delay unit 401 is configured for receiving an input signal CP such as a clock signal from a high speed electronics device, and for generating early and/or late programmably delayed representatives of the input signal (i.e., 412 and 415, respectively). Monitor logic 408 is configured for detecting a phase difference between the input signal CP, and the early and/or late signals to provide a programmable delay to delay unit 401 that correspondingly adjusts the phase of signals 412 and 415. This adjustment of the phase may provide timing for master delay 400 that corresponds to the input signal CP. Master delays, as used for the purposes of timing, are known to those skilled in the art. Examples of typical master delays can be found at the following Micron Technology, Inc. website <http://www.micron.com/content.jsp?path=/Publications/Product+Publications/DesignLine>, and are herein incorporated by reference [www.micron.com](http://www.micron.com).--